OIPE JC112 DEC 03 2004 PATENT & TRADEMARK OFFICE

AF/Ezw

TRANSMITTAL FORM

(to be used for all correspondence after initial filing)

Application No.	09/667,050
Filing Date	September 21, 2000
First Named Inventor	Zohar Bogin
Art Unit	2187
Examiner Name	Kimberly N. McLean-Mayo
Total Number of Pages in This Submission	36
Attorney Docket Number	42390P9415

ENCLOSURES *(check all that apply)*

- [X] Fee Transmittal Form
  - [X] Fee Attached
- [ ] Amendment / Response
  - [ ] After Final
  - [ ] Affidavits/declaration(s)
- [ ] Extension of Time Request
- [ ] Express Abandonment Request
- [ ] Information Disclosure Statement
  - [ ] PTO/SB/08
- [ ] Certified Copy of Priority Document(s)
- [ ] Response to Missing Parts/ Incomplete Application
  - [ ] Basic Filing Fee
  - [ ] Declaration/POA
  - [ ] Response to Missing Parts under 37 CFR 1.52 or 1.53
- [ ] Drawing(s)
- [ ] Licensing-related Papers
- [ ] Petition
- [ ] Petition to Convert a Provisional Application
- [ ] Power of Attorney, Revocation Change of Correspondence Address
- [ ] Terminal Disclaimer
- [ ] Request for Refund
- [ ] CD, Number of CD(s)
- [ ] After Allowance Communication to Group
- [ ] Appeal Communication to Board of Appeals and Interferences
- [X] Appeal Communication to Group **(Appeal Notice, Brief, Reply Brief)**
- [ ] Proprietary Information
- [ ] Status Letter
- [X] Other Enclosure(s) *(please identify below):*

Return receipt postcard

Remarks

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT

Firm or Individual name	Joseph Lutz, Reg. No. 43,765 BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP
Signature	
Date	November 30, 2004

CERTIFICATE OF MAILING/TRANSMISSION

I hereby certify that this correspondence is being deposited with the United States Postal Service on the date shown below with sufficient postage as first class mail in an envelope addressed to: Mail Stop Appeal Brief-Patents, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

Typed or printed name	Marilyn Bass		
Signature		Date	11-30-04

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FEE TRANSMITTAL for FY 2004

Effective 10/01/2004. Patent fees are subject to annual revision.

☐ Applicant claims small entity status. See 37 CFR 1.27.

TOTAL AMOUNT OF PAYMENT ($) 340.00

Complete if Known	
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METHOD OF PAYMENT *(check all that apply)*

☐ Check ☐ Credit card ☐ Money Order ☐ Other ☐ None

☐ Deposit Account

Deposit Account Number: 02-2666

Deposit Account Name: Blakely, Sokoloff, Taylor & Zafman LLP

The Commissioner is authorized to: *(check all that apply)*

☐ Charge fee(s) indicated below ☐ Credit any overpayments

☐ Charge any additional fee(s) or underpayment of fees as required under 37 CFR §§ 1.16, 1.17, 1.18 and 1.20.

☐ Charge fee(s) indicated below, **except for the filing fee** to the above-identified deposit account

FEE CALCULATION

1. BASIC FILING FEE

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
1001	790	2001	395	Utility filing fee	
1002	350	2002	175	Design filing fee	
1003	550	2003	275	Plant filing fee	
1004	790	2004	395	Reissue filing fee	
1005	160	2005	80	Provisional filing fee	

SUBTOTAL (1) ($)

2. EXTRA CLAIM FEES

		Extra Claims		Fee from below		Fee Paid
Total Claims	10 - 29** =	0	x	18.00	=	$0.00
Independent Claims	3 - 5** =	0	x	88.00	=	$0.00
Multiple Dependent					=	

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description
1202	18	2202	9	Claims in excess of 20
1201	88	2201	44	Independent claims in excess of 3
1203	300	2203	150	Multiple Dependent claim, if not paid
1204	88	2204	44	**Reissue independent claims over original patent
1205	18	2205	9	**Reissue claims in excess of 20 and over original patent

SUBTOTAL (2) ($) 0.00

***or number previously paid, if greater, For Reissues, see below*

FEE CALCULATION (continued)

3. ADDITIONAL FEES

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
1051	130	2051	65	Surcharge - late filing fee or oath	
1052	50	2052	25	Surcharge - late provisional filing fee or cover sheet.	
2053	130	2053	130	Non-English specification	
1812	2,520	1812	2,520	For filing a request for *ex parte* reexamination	
1804	920 *	1804	920 *	Requesting publication of SIR prior to Examiner action	
1805	1,840 *	1805	1,840 *	Requesting publication of SIR after Examiner action	
1251	110	2251	55	Extension for reply within first month	
1252	430	2252	215	Extension for reply within second month	
1253	980	2253	490	Extension for reply within third month	
1254	1,530	2254	765	Extension for reply within fourth month	
1255	2,080	2255	1,040	Extension for reply within fifth month	
1404	340	2401	170	Notice of Appeal	
1402	340	2402	170	Filing a brief in support of an appeal	340.00
1403	300	2403	150	Request for oral hearing	
1451	1,510	2451	1,510	Petition to institute a public use proceeding	
1452	110	2452	55	Petition to revive - unavoidable	
1453	1,370	2453	685	Petition to revive - unintentional	
1501	1,370	2501	685	Utility issue fee (or reissue)	
1502	490	2502	245	Design issue fee	
1503	660	2503	330	Plant issue fee	
1460	130	2460	130	Petitions to the Commissioner	
1807	50	1807	50	Prosessing fee under 37 CFR 1.17(q)	
1806	180	1806	180	Submission of Information Disclosure Stmt	
8021	40	8021	40	Recording each patent assignment per property (times number of properties)	
1809	790	1809	395	Filing a submission after final rejection (37 CFR § 1.129(a))	
1810	790	2810	395	For each additional invention to be examined (37 CFR § 1.129(b))	
1801	790	2801	395	Request for Continued Examination (RCE)	
1802	900	1802	900	Request for expedited examination of a design application	

Other fee (specify) _____

* Reduced by Basic Filing Fee Paid

SUBTOTAL (3) ($) 340.00

SUBMITTED BY

Complete (if applicable)

Name *(Print/Type)*	Joseph Lutz	Registration No. *(Attorney/Agent)*	43,765	Telephone	(310) 207-3800
Signature				Date	11-30-04

Based on PTO/SB/17 (10-03) as modified by Blakely, Sokoloff, Taylor & Zafman (wh) 02/10/2004.
SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450

OIPE JC112
DEC 03 2004
PATENT & TRADEMARK OFFICE

Attorney's Docket No.: 42390.P9415

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application for:	)
	) Examiner: Kimberly N. McLean-Mayo
Zohar Bogin et al.	)
	) Group Art Unit: 2187
Application No. 09/667,050	)
	)
Filed: September 21, 2000	)
	)
For: REMAPPING I/O DEVICE ADDRESSES INTO HIGH MEMORY USING GART	)
	)

APPEAL BRIEF

Mail Stop Appeal Brief - Patent
Commissioner for Patents
P.O. 1450
Alexandria, VA 22313-1450

Dear Sir:

Applicants submit the following Appeal Brief pursuant to 37 C.F.R. §41.37(c) for consideration by the Board of Patent Appeals and Interferences. Applicants also submit herewith a check in the amount of $340.00 to cover the cost of filing the opening brief as required by 37 C.F.R. § 1.17(f). Please charge any additional amount due or credit any overpayment to deposit Account No. 02-2666.

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I. REAL PARTY IN INTEREST

Zohar Bogin and Jeffrey L. Rabe, the parties named in the caption, transferred their rights to that which is disclosed in the subject application through an assignment recorded on December 5, 2000 (011353/0026) in the patent application to Intel Corporation, of Santa Clara, California. Thus, as the owner at the time the brief is being filed, Intel Corporation, of Santa Clara, California is the real party in interest.

II. RELATED APPEALS AND INTERFERENCES

There are no related appeals or interferences which will affect or be affected by the outcome of this appeal.

III. STATUS OF CLAIMS

Claims 8, 9, 12-15, 17, 19-21 and 30-32 are pending and rejected in this application. Applicants hereby appeal the rejection of all pending claims.

IV. STATUS OF AMENDMENTS

The claims are amended in accordance with the Response Amendment fax filed on April 2, 2003, wherein Claims 15, 17 and 19 were amended. The claim amendments requested in the Response Amendment fax filed on April, 2003 regarding Claims 15, 17 and 19 were entered.

V. SUMMARY OF THE CLAIMED SUBJECT MATTER

The pending claims relate to a method and apparatus for remapping input/output (I/O) device addresses into high memory using a graphics address relocation table (GART). As recited by independent Claim 8, a conversion table (27) is used to translate a first address from a graphics controller (26) to a second address of a memory (24). As illustrated with reference to FIG. 2 of Applicants' Specification, the conversion table (27) is shared between bus controller (29), which is coupled to an I/O bus (28), such as PCI bus, and graphics controller (GC) (26). As recited by Claim 8, the conversion table (27) is used to translate a third address from the bus controller (29) to a fourth address to the memory (24). As recited by Claim 8, the second address has a greater number of bits than the first address, and the fourth address has a greater number of

bits than the third address to remap I/O device and graphics addresses into high memory (above four gigabytes (GB)).

In the embodiment illustrated in FIG. 2, the 32-bit register width conventionally used to access memory 24 is expanded to 36 bits using graphics address relocation table (GART) 27 to enable addressing to reach a full 64 GB of memory 24.

Independent Claims 15 and 19 recite:

> a translation lookaside buffer (43) coupled to an input register (41) and an output register (44).

As shown in FIGS. 3 and 4 of Applicants' Specification, control logic 39 coupled to the translation lookaside buffer 43, the input register 42 and the output register 44 compares a first portion (U1) of an initial address for a bus controller 29 and the input register 41 with entries in the translation lookaside buffer 43. In the embodiment illustrated, when a matching entry is found, control logic 29 combines a first value (U21-U26) associated with the matching entry with a second portion (L1) of the initial address to form a first translated address having a greater number of bits than the initial address and hold the first translated address in output register 44.

As shown in FIG. 4, the control logic 39 is further to access a table 42 in memory 14 if the matching entry is not found to find a second value (U201-U207) in the table 42 associated with the first portion (U1) and combine the second value (U2) with the second portion (L1) to form a second translated address having a greater number of bits than the initial address and hold the second translated address in the output register 44.

Independent Claim 30 recites:

> an address translator (39) having a first interface to couple to a memory controller (25), a second interface to couple to a graphics controller (26), a third interface to couple to a bus controller (29), and a table (43) of entries, each entry having a first portion (U11-U16) and a second portion (U21-U26).

As recited by independent Claim 30:

> a translation control circuit (38) is coupled to the address translator (39) to program the entries in the address translator (39);
>
> wherein the address translator (39) is to translate an address on the third interface (bus controller (29)) into a first address on the first interface (memory controller (25)) having a greater number of bits than the address on the third interface.

Accordingly, as recited by the claimed invention and illustrated with reference to FIG. 2 of Applicants' Specification, by coupling bus controller 29 to GART 27, and modifying the expanded GART 27 to accept an interface to a device other than graphics controller 26, bus controller 29 can be permitted to access memory outside the normal 4 GB range that the bus controller is normally limited to. Thus, devices on PCI bus 28 can transfer data directly to any part of the full memory range of 64 GB, without an intermediate transfer operation performed by software. (*See*, Applicants' Specification, pg. 4, line 21 - pg. 5, line 2.)

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

The grounds of rejection involved in this appeal are as follows:

Are Claims 8-9, 12-14 and 30-32 unpatentable under 35 U.S.C. §103(a) as being unpatentable over Jeddeloh, U.S. Patent No. 6,477,623 ("Jeddeloh") in view of Alpert, U.S. Patent No. 5,802,605 ("Alpert")?

Are Claims 15 and 17 unpatentable under 35 U.S.C. §103(a) as being unpatentable over Jeddeloh in view of Alpert and further in view of Dixit, U.S. Patent No. 5,574,877 ("Dixit")?

Are Claims 19-21 unpatentable under 35 U.S.C. §103(a) as being unpatentable over Jeddeloh in view of Dixit?

VII. ARGUMENT

A. Overview of the Cited References

1. Overview of Jeddeloh Reference

Jeddeloh describes a method for providing a graphics controller embedded in a core logic unit to facilitate high-bandwidth communications between the graphics controller and other system components, such as the processor and system memory. As described in the Background of Jeddeloh:

> . . . data transfers between processor and graphics controller, and between graphics controller and system memory are presently constrained by the bandwidth of the busses and/or data channels that couple these system components together. (col. 1, lines 57-61.)

To solve this problem, Jeddeloh teaches:

> . . . because the data paths connecting graphics controller 140 and other devices to switch 124 do not cross chip boundaries, they are not

> constrained by the pinout limitations of semiconductor chips. Hence, these data paths can be considerably wider than busses that typically couple computer system components together. These wide data paths can be useful in transferring the high-bandwidth data received from clocked interfaces on SyncLink or Rambus memory devices. (col. 6, lines 1-9.)

To further improve the high-bandwidth communication between the graphics controller and other system components, Jeddeloh describes GART table 202 as illustrated in FIG. 3:

> GART table 202 performs address translation on-the-fly as a data transfer traverses switch 124. If an address does not fall within the reserved range of address, the data transfer is allowed to proceed. On the other hand, if the address falls within the reserved range of addresses, the data transfer is delayed (perhaps by a clock cycle) so that the address translation can take place. Next, the data transfer is allowed to proceed using the translated address. This differs from conventional systems that place a GART table lookup in the path of all addresses. (col. 6, lines 51-61.)

As further described by Jeddeloh:

> the present invention tests each destination address to see if it falls within the reserved range of addresses, and if so, performs the address translation. This differs from conventional systems in which GART tables are used to translate only destination addresses originating from an off-chip graphics controller. This added flexibility allows other devices such as a processor attached to a processor interface 126 or a direct memory access (DMA) device attached to bus interface 130 to directly access graphics data stored in system memory. (col. 6, lines 41-50.)

However, the address translation using a GART table 202, as taught by Jeddeloh, is based on the bus or register width, such as, for example, conventional 32-bit registers to provide a 32-bit address range, which allows direct addressing of up to 4 gigabytes (GB) of memory. In fact, the number of bits of the translated address provided by the GART translation mechanism, as taught by Jeddeloh, will have the same number of bits as the received address, whether the address does or does not fall within the reserved address range for graphics applications.

2. Overview of Alpert Reference

Alpert teaches a processor paging mechanism and the extension of the paging mechanism to provide a physical address size selection (e.g., 36-bits) and page size selection. As described by Alpert:

> The address translator translates from a standard 32-bit linear address for compatibility with previous architectures. However, the translator can translate to a physical address that is larger than the linear address; i.e., greater than 32-bits (e.g., 36 bits). (col. 3, lines 35-39.)

As illustrated with reference to FIG. 10 of Alpert, the address translation referred to is the address translation performed using the page unit 110 of a microprocessor 100. Alpert teaches an address translator which enables a physical address size selection and a page size selection. Conventionally, page sizes are generally 4K-bytes, for example, as described in Alpert:

> For example, the page size for the Intel 80386 and i486 microprocessor is 4K-bytes. (col. 2, lines 32-33.)

FIGS. 2 and 8 of Alpert illustrate the type 3 extended addressing mode, as referred to in Table 2 of Alpert, which provides a 36-bit physical address space with a 4K-byte page. As described by Alpert:

> For the small page size and extended physical memory, three levels of tables are used. These three levels include a directory pointer table 20, a page table directory 22 and a page table 24. . . . In order to access an operand, a control register 40 holds a value that points to the address of a particular directory pointer table 20 in memory. . . .
>
> The pointer field 42 points to a particular pointer 30 in the directory pointer table 20 that is selected by the control register 40. . . . The selected pointer 30 is applied to select a particular page table directory 22. Once the page table directory 22 is selected, a directory field 44 of the linear address selects a particular page directory entry 32. The selected page directory entry 32 points to one of the plurality of page tables 24. A page field 46 within the linear address selects a particular page table entry 34 in the selected page table 24. The selected page table entry 34 selects a page frame 36 in physical memory. The offset field 48 in the linear address points to an operand 38 in the specified page frame 36 in physical memory. (col. 8, lines 16-51.) (Emphasis added.)

Based on the cited passage above and the entire specification of Alpert, the teachings of Alpert are strictly limited to the modification of the processor's paging mechanism.

This paging mechanism is limited to the processor since the processor executes all program instructions and translates addresses issued by the executing program instructions. Since the remaining components of a computer system do not execute program instructions, computer systems limit paging and address translation to the processor. Hence, the teachings of Alpert are strictly limited to modification of the processor paging mechanism to enable physical address size selection and page size selection.

3. Overview of Dixit Reference

Dixit is similar to Alpert and provides a modification to the processor paging mechanism, wherein the translation lookaside buffers (TLBs) have at least two page frame numbers (PFN) associated with each tag (virtual page number). As described within the Background of Dixit:

> . . . the TLB mechanism is especially useful in systems where multiple programs run, since each program typically will elect to start at address zero. The TLB allows the mapping of separate programs to separate areas of memory, while each program thinks it is operating in the same space, starting at zero. (*See*, col. 1, lines 9-15.)

As further described:

> The TLB is essentially a table which is stored in memory. Like other aspects of memory, the TLB is at least partially stored on the microprocessor chip itself in the form of a cache memory. (col. 1, lines 28-31.)

Accordingly, Dixit teaches expansion to the TLB mechanism, such that each TLB has:

> . . . at least two page frame numbers (PFN) associated with each tag (virtual page number). Thus, a match will produce two possible physical page frame numbers. The selection between these two is controlled by a bit provided directly from the virtual address, without translation. This bit is preferably the least significant bit of the virtual page number, or the first bit after the physical offset.
>
> The structure of the present invention effectively doubles the capacity of the TLB without doubling the number of tags. Although the virtual space covered by each tag, or VPN is necessarily restricted to two contiguous areas, the invention allows these two contiguous areas to be mapped to completely different regions of the physical address space. In addition to limiting the number of tags required, the number of comparators required is also similarly limited, with only the number of

physical page frame numbers stored being required to double. (col. 2, lines 22-40.)

Hence, like or similar to Alpert, the teachings of Dixit are strictly limited to modifications to the processor paging mechanism, which as clearly indicated by Dixit, relies on such mechanisms, such as the translation lookaside buffer, which is at least partially stored in the microprocessor chip itself in the form of cache memory and, generally not available to off-chip devices.

B. Rejection of Claims 8-9 and 12-14 as Obvious Over Jeddeloh in View of Alpert

The Examiner rejected all pending claims, including Claims 8-9 and 12-14 under 35 U.S.C. §103(a) as being unpatentable over Jeddeloh in view of Alpert.

1. Errors of Law and Fact in the Rejection

For the reasons provided below, the Examiner has failed to establish a *prima facie* case of obviousness in view of the references of record. The Federal Circuit Court of Appeals in In re Rijckaert, 9 F.3d 1531, 28 U.S.P.Q. 2d 1955 (Fed. Cir. 1993) held that:

> In rejecting claims under 35 U.S.C. § 103, the examiner bears the initial burden of presenting a *prima facie* case of obviousness. . . . "A *prima facie* case of obviousness is established when the teaching from the prior art itself would appear to have suggested the claimed subject matter to a person of ordinary skill in the art.". . . If the examiner fails to establish a *prima facie* case, the rejection is improper and will be overturned. (Emphasis added.) 9 F.3d at 1532, 28 U.S.P.Q. 2d at 1956.

The Examiner recognizes the lack of any teaching or suggestion within Jeddeloh regarding the expansion of a translator physical address range. As a result, cites Alpert. According to the Examiner, Alpert teaches a concept of using a conversion table (page table) to translate an initial address to a translated address wherein the translated address has a greater number of bits than the initial address. According to the Examiner,

> . . . it would have been obvious to one or ordinary skill in the art at the time the invention was made to use the teachings of Alpert with the teachings of Jeddeloh for the desirable purpose of expanding the addressing capability of a system by allowing the system to access a larger amount of physical memory and thereby improve the performance of the system. (*See*, pp. 2-3 of Final Office Action, mailed July 14, 2004.)

Applicants respectfully disagree with the Examiner's contention. Applicants respectfully submit that the Examiner's contention that Alpert teaches a conversion table (page table) to translate an initial address to a translated address, wherein the translated address has a greater number of bits than the initial address, fails to comply with the legal requirements as mandated by M.P.E.P. §2141. As recited by M.P.E.P. §2141, the references must be considered as a whole and must suggest the desirability and thus the obviousness of making the combination.

Here, Alpert teaches an address translator which enables a physical address size selection and a page size selection. Conventionally, page sizes are generally 4K-bytes, for example, as described in Alpert:

> . . . the page size for the Intel 80386 and i486 microprocessor is 4K-bytes. (col. 2, lines 32-33.)

FIGS. 2 and 8 of Alpert illustrate the type 3 extended addressing mode, as referred to in Table 2 of Alpert, which provides a 36-bit physical address space with a 4K-byte page. As described with reference to FIG. 2 of Alpert:

> For the small page size and extended physical memory, three levels of tables are used. These three levels include a directory pointer table 20, a page table directory 22 and a page table 24. (col. 8, lines 16-19.)

In addition, to provide the components for accessing the three levels of tables to implement the small page size and extended physical memory address:

> A linear address 41 for a small page size is divided into a pointer field 42, a directory field 44, a page field 46 and an offset field 48. (col. 8, lines 33-35.)

As is further described with reference to col. 8 of Alpert, as well as cols. 10 and 11, the process for supporting the small page size and extended physical address, as taught by Alpert, is a rather complicated process requiring three levels of tables and a linear address that is divided into four different fields. Applicants respectfully submit that this complicated process does not merely describe a conversion table where a translated address has a greater number of bits than the initial address, as suggested by the Examiner.

Furthermore, since most architecture designs are based on the presumption that only the processor executes program instructions, system architects limit address translation and

paging to the processor without providing access to such features to off-chip components. Hence, the complex physical address size selection and page size selection process taught by Alpert is solely limited to the processor paging mechanism. Accordingly, Applicants respectfully submit that Alpert is devoid of any teachings with regards to providing physical address translation and paging to off-chip components, such as, for example, graphics controllers and I/O devices.

Hence, the teachings of both Jeddeloh and Alpert would not suggest modification of the address translation using the GART table of Jeddeloh to extend the physical address space, as recited by the claimed invention, since the teachings of Jeddeloh are specifically limited to addressing the following problem described in the Background of Jeddeloh:

> Data transfers between processor and graphics controller, and between graphics controller and system memory are presently constrained by the bandwidth of the busses and their data channels that couple these components together. (col. 1, lines 56-60.)

As specifically indicated in the Background of Jeddeloh, what is needed is a computer system architecture that facilitates high-bandwidth data transfers between a graphics controller and other system components. (*See*, col. 2, lines 11-13.) To achieve this goal, Jeddeloh teaches data paths, which connect the graphics controller and other devices to switch 124 (FIG. 2) to have a greater width than the busses typically couple computer system components together.

In other words, the teachings of Jeddeloh are directed to providing high-bandwidth communications and not directed to physical address range limitations caused by bus and register widths. Accordingly, Applicants respectfully submit that the combined teachings of Jeddeloh in view of Alpert would not have suggested the claimed invention to one of ordinary skill in the art, as required to establish a *prima facie* case of obviousness. Id.

Furthermore, case law has established that obviousness cannot be established by combining the teachings of the prior art to produce the claimed invention absent the teaching or suggestion supporting such combination. ACS Hospital Sys., Inc. v. Montefiore Hospital, 732 F.2d. 1572, 1577, 221 U.S.P.Q. 929, 933 (Fed. Cir. 1984). Moreover, one cannot find obviousness through hindsight to construct a claimed invention from elements of the prior art. In re Warner, 379 F.2d 1011, 1016, 154 U.S.P.Q. 173, 177 (C.C.P.A. 1967).

Here, Jeddeloh is completely devoid of, and fails to teach or suggest, expansion of the physical address range. Instead of modification to a translator physical address range, the teachings of Jeddeloh are specifically limited to avoiding the bandwidth constraints imposed on data transfers between the processors and graphics controllers due to busses and/or data channels that couple these components together. (*See*, col. 1, lines 57-61.) The only mention of address translation within Jeddeloh occurs at col. 6, wherein it is indicated that GART table 202 performs address translation on-the-fly as data transfer traverse switch 124 such that addresses that fall within a reserved range are delayed so that address translation can take place. (*See*, col. 6, lines 51-61.) In fact, Jeddeloh fails to teach or suggest how this address translation is performed and simply refers to the address translation without providing any details as to how such translation is performed.

Conversely, Alpert is directed to modification of the paging mechanism of a processor to enable selection of a physical address range size and page size selection, which requires use of processor control registers, three levels of tables and various configurations of a linear address to include a pointer field 46, directory field 44, page field 46 and offset field 48 to provide the physical address range size and page size, as shown in FIGS. 2, 8, 10 and the flowcharts in FIGS. 11 and 12 of Alpert.

Applicants respectfully submit that one skilled in the art would not have a motivation for the modification of Jeddeloh in view of Alpert due to the lack of any mention of the address translation provided by the GART table taught by Jeddeloh and that the complex physical address size selection and page size selection process taught by Alpert is solely limited to the processor paging mechanism. Applicants respectfully submit that both the references of Jeddeloh and Alpert, as well as the skill in the art, would not provide a suggestion or motivation for combining the reference teachings, as required to establish a *prima facie* case of obviousness.

Accordingly, Applicants respectfully submit that the Examiner fails to establish that it would be obvious to combine the missing elements provided by Alpert with the teachings of Jeddeloh. Consequently, Applicants respectfully submit that Applicants' claimed invention could only be arrived at through inappropriate hindsight.

Moreover, Applicants respectfully submit that the modification of Jeddeloh in view of Alpert would require a change to the principle of operation of Jeddeloh. As indicated by the Federal Circuit:

> If the proposed modification or combination of the prior art would change the principle of operation of the prior art invention being modified, then the teachings of the references are not sufficient to render the claims *prima facie* obvious. In re Ratti, 270 F.2d 810, 123, U.S.P.Q. 349 (C.C.P.A. 1959).

Applicants respectfully submit that modification of the GART table and address translation mechanism, as taught by Alpert, would require substantial modification to the north bridge of Jeddeloh to provide the various control registers, the three levels of tables for the small page size and extended physical address, the four field linear address and logic required to perform the extended addressing, as taught by Alpert. Furthermore, the off-chip controllers would require modification to populate the various control registers to direct the chipset to perform the extended address translation taught by Alpert. Accordingly, Applicants respectfully submit that the teachings of the combinations of Jeddeloh in view of Alpert are not sufficient to render the claims *prima facie* obvious. Id.

Accordingly, Applicants respectfully submit that the combined teachings of Jeddeloh in view of Alpert would not have suggested the claimed invention to one of ordinary skill in the art, as required to establish a *prima facie* case of obviousness. Id. Hence, a *prima facie* case of obviousness has not been established and the rejection is erroneous and should be overturned.

2. Specific Limitations Not Described in the Prior Art

Independent Claim 8 recites the following claim feature, which is neither taught nor suggested by either Jeddeloh, Alpert or the references of record:

> using a conversion table to translate a first address from a graphics controller to a second address to a memory; and
>
> using the conversion table to translate a third address from a bus controller to a fourth address to the memory;
>
> wherein the second address has a greater number of bits than the first address and the fourth address has a greater number of bits than the third address. (Emphasis added.)

3. Explanation Why Such Limitations Render the Claims Non-obvious Over the Prior Art

As described within the Background of Alpert:

> microprocessors designed to use virtual memory effectively extend main memory space into secondary memory space. Typically, virtual

memory microprocessors use a technique, such as paging or segmentation, or both, to simulate a larger memory. (col. 1, lines 25-30.)

Virtual memory as described by Alpert and known to those skilled in the art, provides a technique to effectively expand the capacity of main memory, or volatile memory, from the perspective of the application programs. Address translation to support virtual memory in computer systems is generally limited to a processor address translation and paging mechanism, since the processor is generally responsible for executing program instructions. Accordingly, when an application program is executing, the processor's paging mechanism automatically performs the address translation for address references issued by the executing application program instructions.

In operation, when a graphics application requires allocation of a portion of main memory for the graphics adapter's use, it issues a request to an operating system (OS) memory allocation routine, which assigns a portion of main memory, referred to as the "graphics aperture." Generally, the request for a large block of main memory results in the allocation of a series of non-contiguous pages to yield the requested block size, such that from the graphics adapter's perspective, system memory is allocated as a continuous block according to the requested size.

Once the portion of main memory is allocated, the OS returns a 32-bit linear memory start address (above the top of memory) to the graphics application and sets up a series of page table entries, as well as translation lookaside buffers (TLB) that will translate addresses that fall within the graphics aperture to the appropriate pages of main memory. Unfortunately, this technique presumes that the memory accesses to the graphics aperture will come from application program instructions, such as a graphics application executing within the processor, which therefore implicitly takes advantage of the processor's paging mechanism.

However, when the graphics adapter attempts to access the graphics aperture, neither the graphics adapter nor the chipset between the graphics controller and main memory know where the processing page tables are in memory and therefore cannot take advantage of the processor's address translation mechanism. To solve this problem, software is used to build a graphics address relocation table (GART) in memory. As taught by Jeddeloh:

Graphics address relocation table (GART table) 202 is used to translate addresses from a reserved range of graphics addresses into

addresses containing graphics data that are scattered throughout system memory. (col. 6, lines 17-21.)

In contrast to conventional GART usage, Jeddeloh teaches that:

> . . . the present invention tests each destination address to see if it falls within the reserved range and if so performs the address translation. This differs from conventional systems in which GART tables are used to translate only destination addresses originating from an off-chip graphics controller. (col. 6, lines 41-46.) (Emphasis added.)

However, the address translation using the GART table 202 of Jeddeloh limits the graphics devices, as well as other components coupled to switch 124, to a 32-bit physical address range and therefore the components cannot directly address more than 4 GB of memory. Yet, the teachings of Jeddeloh are not concerned with being limited to directly addressing up to 4 GB of memory based on 32-bit wide conventional registers. The teachings of Jeddeloh are directed to improving high-bandwidth communication between the graphics controller and other system components, as illustrated in FIG. 2 of Jeddeloh, which are generally constrained by the bandwidth of busses and/or data channels that couple these system components together. (*See*, col. 1, lines 57-61 of Jeddeloh.)

As a result, Jeddeloh teaches data paths connecting the graphics controller 140 and other devices to switch 124 that have considerably wider path widths than busses that typically couple system components together. These wide data path widths can be useful in transferring the high-bandwidth data received from clock interfaces on SyncLink or Rambus memory devices. (*See*, col. 6, lines 1-11.) Hence, Jeddeloh is completely absent of any teaching or suggestion regarding the limitation of such peripheral devices to a 32-bit physical address range.

Furthermore, the 32-bit physical address range is only a limitation for computer systems that provide a memory capacity that is greater than 4 GB of memory. As described by Alpert:

> Although large by past standards, a 4 Gbyte limit on physical memory is becoming a limitation, particularly for very larger servers. (col. 3, lines 15-17.)

Applicants respectfully submit that modifying Jeddeloh in view of Alpert would result in a modification of the processor paging mechanism of the processors of the system

taught by Jeddeloh, assuming the system of Jeddeloh was a server based system with a physical memory capacity exceeding 4 GB. Applicants' statement is based on the fact that Jeddeloh is devoid of any teachings as to how address translation is performed if an address falls within the reserved range of addresses. As indicated by Jeddeloh:

> If the address falls within the reserved range of addresses, the data transfer is delayed (perhaps by a clock cycle) so that the address translation can take place. (col. 6, lines 54-57.)

Conversely, Alpert is directed to modification of the paging mechanism of a processor to enable selection of a physical address range size and page size selection, which requires use of processor control registers, three levels of tables and various configurations of a linear address to include a pointer field 46, directory field 44, page field 46 and offset field 48 to provide the physical address range size and page size, as shown in FIGS. 2, 8, 10 and the flowcharts in FIGS. 11 and 12 of Alpert.

Applicants respectfully submit that using the teachings of Alpert with the teachings of Jeddeloh, as suggested by the Examiner, would result in the system as taught by Jeddeloh in which the processor paging mechanism is altered without any modification to the address translation using the GART table. As indicated above, the inability of off-chip devices to make use of the processor paging mechanism, and specifically, graphics controllers, led to the creation of the GART tables to perform such translation for graphics devices.

Therefore, since the teachings of Alpert are strictly limited to modification of the processor paging mechanism, Applicants respectfully submit that the combination of the teachings of Jeddeloh in view of Alpert would be limited to the modification of the processor paging mechanism of processors 112, 114 and 116, as illustrated in FIG. 1 of Jeddeloh. However, the case law is clear in establishing that "to establish *prima facie* obviousness of a claimed invention, all the claim limitations must be taught or suggested by the prior art." In re Royka, 490 F.2d 981, 180 U.S.P.Q. 580 (CCPA 1974).

Here, the combination or modification of Jeddeloh in view of Alpert would fail to teach or suggest address translation from a graphics controller and a bus controller using the same conversion table where a number of bits of the translated address is greater than a number of bits of the initial address, as recited by the claimed invention. Hence, the Examiner fails to

establish a *prima facie* case of obviousness since the combination or modification of Jeddeloh in view of Alpert fails to teach all limitations of the claimed invention. Id.

Furthermore, for at least the reasons indicated above, the Examiner also fails to illustrate a motivation within either Jeddeloh, Alpert or the skill in the art to modify Jeddeloh, as suggested by the Examiner in view of Alpert. Accordingly, Applicants respectfully submit that the features of the claimed invention can only be arrived at through inappropriate hindsight.

Therefore, Applicants respectfully submit that a *prima facie* case of obviousness is not established and therefore, the rejection is erroneous and should be overturned. Accordingly, Applicants respectfully request that the §103(a) rejection of Claims 8-9 and 12-14 be overturned.

C. Rejection of Claims 15 and 17 as Obvious Over Jeddeloh in View of Alpert and Further in View of Dixit

1. Errors of Law and Fact in the Rejection

The Examiner has made the same errors as described previously with respect to the rejected Claims 8, 9 and 12-14. In addition, the Examiner has failed to show a teaching or suggestion to modify Jeddeloh in view of Alpert and further in view of Dixit.

The Examiner rejected Claims 15 and 17 under 35 U.S.C. §103(a) as being unpatentable over Jeddeloh in view of Alpert and further in view of Dixit. The Examiner recognizes the lack of any teaching or suggestion within Jeddeloh regarding the expansion of a translator physical address range. As a result, the Examiner cites Alpert. In addition, the Examiner recognizes the lack of any teaching or suggestion within Jeddeloh regarding the input and output registers, as recited by the claimed invention. As a result, the Examiner cites Dixit.

Case law has established that obviousness cannot be established by combining the teachings of the prior art to produce the claimed invention absent the teaching or suggestion supporting such combination. ACS Hospital Sys., Inc. v. Montefiore Hospital, 732 F.2d. 1572, 1577, 221 U.S.P.Q. 929, 933 (Fed. Cir. 1984). Also, one cannot find obviousness through hindsight to construct a claimed invention from elements of the prior art. In re Warner, 379 F.2d 1011, 1016, 154 U.S.P.Q. 173, 177 (C.C.P.A. 1967).

According to the Examiner, Alpert teaches a concept of using a conversion table (page table) to translate an initial address to a translated address wherein the translated address has a greater number of bits than the initial address. However even if Alpert discloses using a

conversion table (page table) to translate an initial address to a translated address wherein the translated address has a greater number of bits than the initial address, the Examiner fails to establish that it would be obvious to combine the missing elements provided by Alpert with the teachings of Jeddeloh.

Here, Dixit is similar to Alpert and provides a modification to the processor paging mechanism, wherein the translation lookaside buffers (TLBs) have at least two page frame numbers (PFN) associated with each tag (virtual page number). Analogous to Alpert, the teachings of Dixit are strictly limited to modifications to the processor paging mechanism, which as clearly indicated by Dixit, relies on such mechanisms, such as the translation lookaside buffer, which is at least partially stored in the microprocessor chip itself in the form of cache memory and, generally not available to off-chip devices. (*See*, col. 1, lines 28-31.)

Applicants respectfully submit that the failure of both Alpert and Dixit to teach anything other than modification of a processor paging and translation mechanism prohibits the Examiner from establishing a teaching or suggestion to support the combination of Jeddeloh in view of Alpert and further in view of Dixit to produce the claimed invention. Accordingly, Applicants respectfully submit that Applicants' claimed invention could only be arrived at through inappropriate hindsight. Hence, Applicants respectfully submit that the Examiner fails to establish that it would be obvious to combine the missing elements provided by Alpert in view of Dixit with the teachings of Jeddeloh.

Therefore, a *prima facie* case of obviousness has not been established and the rejection is erroneous and should be overturned.

2. Specific Limitations Not Described in the Prior Art

Independent Claim 15 recites the following claim feature, which is neither taught nor suggested by either Jeddeloh, Alpert, Dixit or the references of record

> wherein the control logic is to compare a first portion of an initial address from a bus controller in the input register with entries in the translation lookaside buffer; and if a matching entry is found, to combine a first value associated with the matching entry with a second portion of the initial address to form a first translated address having a greater number of bits than the initial address and hold the first translated address in the output register;
>
> wherein the control logic is further to access a table in memory if the matching entry is not found, find a second value in the table associated

with the first portion, combine the second value with the second portion to form a second translated address having a greater number of bits than the initial address, and hold the second translated address in the output register. (Emphasis added.)

3. Explanation Why Such Limitations Render the Claims Non-obvious Over the Prior Art

The case law is quite clear in establishing that the combination of references cited by an Examiner must teach each and every feature of the claimed invention to sustain a *prima facie* case of obviousness. In re Royka, 490 F.2d 981, 180 U.S.P.Q. 580 (CCPA 1974). Here, the Examiner recognizes Jeddeloh's failure to teach expansion of the physical address range. In addition, the Examiner recognizes the lack of any teaching or suggestion within Jeddeloh regarding the input and output registers, as recited by the claimed invention. As a result, the Examiner cites Dixit.

In contrast to modification of a processor paging mechanism (Dixit) or modification of a translator physical address range (Alpert), the teachings of Jeddeloh are specifically limited to avoiding the bandwidth constraints imposed on data transfers between processors and graphics controllers due to busses and/or data channels that couple these components together. (*See*, col., lines 57-61.) Accordingly, the Examiner cites Alpert to teach expansion of a physical address range.

However, as indicated above, the claimed invention recites expansion of the physical range for translation of a physical address received from a bus controller. Conversely, as indicated above, the teachings of Alpert and Dixit are strictly limited to the processor paging mechanism. As repeatedly described above, system architecture design provides a paging and translation mechanism within the processor since the processor is responsible for executing programmed instructions and performing address translation using the processor's paging mechanism for issued address references from executing instructions.

Furthermore, Applicants respectfully submit that the combination of Jeddeloh in view of Alpert and further in view of Dixit, fail to teach the control logic to access a table in memory if the matching entry is not found to form the second translated address having a greater number of bits than the initial address. As described within Jeddeloh:

> If an address does not fall within the reserved range of addresses, the data transfer is allowed to proceed. On the other hand, if the address falls within the reserved range of addresses, the data transfer is delayed

(perhaps by a clock cycle) so that the translation can take place. (col. 6, lines 40-41.) (Emphasis added.)

Conversely, the features of the claimed invention do not limit the address translation of an address received from a bus controller to a reserved range of addresses. As recited by the claimed invention, if a matching entry is not found for any address received from a bus controller, a table in memory is used to find a second value to form the second translated address. Hence, the Examiner fails to establish obviousness since the combination or modification of Jeddeloh in view of Alpert and further in view of Dixit fails to teach all limitations of the claimed invention. Id.

Furthermore, for at least the reasons indicated above, the Examiner also fails to illustrate a motivation within either Jeddeloh, Alpert, Dixit or the skill in the art to modify Jeddeloh, as suggested by the Examiner in view of Alpert and further in view of Dixit. Accordingly, Applicants respectfully submit that the features of the claimed invention can only be arrived at through inappropriate hindsight.

Therefore, Applicants respectfully submit that a *prima facie* case of obviousness is not established and therefore, the rejection is erroneous and should be overturned. Accordingly, Applicants respectfully request that the §103(a) rejection of Claims 15 and 17 be overturned.

D. Rejection of Claims 19-21 as Obvious Over Jeddeloh in View of Dixit

1. Errors of Law and Fact in the Rejection

The Examiner has made the same errors as described previously with respect to the rejected Claims 8, 9, 12-15 and 17. In addition, the Examiner has failed to show a teaching or suggestion to modify Jeddeloh in view of Alpert and further in view of Dixit.

The Examiner rejected Claims 19-21 under 35 U.S.C. §103(a) as being unpatentable over Jeddeloh in view of Alpert and further in view of Dixit. The Examiner recognizes the lack of any teaching or suggestion within Jeddeloh regarding the expansion of a translator physical address range. As a result, the Examiner cites Alpert. In addition, the Examiner recognizes the lack of any teaching or suggestion within Jeddeloh regarding the input and output registers, as recited by the claimed invention. As a result, the Examiner cites Dixit.

Case law has established that obviousness cannot be established by combining the teachings of the prior art to produce the claimed invention absent the teaching or suggestion supporting such combination. ACS Hospital Sys., Inc. v. Montefiore Hospital, 732 F.2d. 1572, 1577, 221 U.S.P.Q. 929, 933 (Fed. Cir. 1984). Also, one cannot find obviousness through hindsight to construct a claimed invention from elements of the prior art. In re Warner, 379 F.2d 1011, 1016, 154 U.S.P.Q. 173, 177 (C.C.P.A. 1967).

Here, the Examiner cites Alpert, which according to the Examiner, teaches using a conversion table (page table) to translate an initial address to a translated address wherein the translated address has a greater number of bits than the initial address. However even if Alpert discloses physical address range expansion, the Examiner fails to establish that it would be obvious to combine the missing elements provided by Alpert with the teachings of Jeddeloh.

Dixit is similar to Alpert and provides a modification to the processor paging mechanism, wherein the translation lookaside buffers (TLBs) have at least two page frame numbers (PFN) associated with each tag (virtual page number). Hence, like or similar to Alpert, the teachings of Dixit are strictly limited to modifications to the processor paging mechanism, which as clearly indicated by Dixit, relies on such mechanisms, such as the translation lookaside buffer, which is at least partially stored in the microprocessor chip itself in the form of cache memory and, generally not available to off-chip devices.

Accordingly, Applicants respectfully submit that the Examiner fails to establish that it would be obvious to combine the missing elements provided by Alpert in view of Dixit with the teachings of Jeddeloh. Accordingly, Applicants respectfully submit that Applicants' claimed invention could only be arrived at through inappropriate hindsight. Consequently, a *prima facie* case of obviousness has not been established and the rejection is erroneous and should be overturned.

2. Specific Limitations Not Described in the Prior Art

Independent Claim 19 recites the following claim feature, which is neither taught nor suggested by either Jeddeloh, Alpert, Dixit or the references of record:

a processor;
a memory;
a graphics controller;
a bus controller;

an input-output controller coupled to the processor, memory, graphics controller and bus controller, the input-output controller including:

a translation lookaside buffer coupled to an input register and an output register;

control logic coupled to the translation lookaside buffer, the input register, and the output register;

wherein the control logic is to compare a first portion of a first initial address from the bus controller in the input register with entries in the translation lookaside buffer; and if a first matching entry is found, to combine a first value associated with the first matching entry with a second portion of the first initial address to form a first translated address having more bits than the first initial address and hold the first translated address in the output register. (Emphasis added.)

3. Explanation Why Such Limitations Render the Claims Non-obvious Over the Prior Art

The Examiner fails to illustrate that the combination or modification of Jeddeloh in view of Alpert and further in view of Dixit teaches or suggests each of the recited features of the claimed invention. However, the case law is clear in establishing that "to establish *prima facie* obviousness of a claimed invention, all the claim limitations must be taught or suggested by the prior art." In re Royka, 490 F.2d 981, 180 U.S.P.Q. 580 (CCPA 1974).

Here, the claimed invention recites an input-output (I/O) controller coupled to the processor, memory, graphics controller and bus controller. Conversely, Jeddeloh:

> North bridge 102 additionally includes graphics controller 140 which contains special purpose circuitry for performing graphics computations. This allows graphics computations to be off-loaded from processors 112, 114 and 116. For example, in one embodiment of the present invention, graphics controller 140 includes circuitry to perform graphics computations for representing two-dimensional and three-dimensional objects. Note that graphics controller 140 is coupled directly to switch 124 and does not pass through any intervening interface or bus that introduce bandwidth limitations. (col. 3, lines 57-67.) (Emphasis added)

Based on the cited passage above, Jeddeloh clearly requires a graphics controller embedded in a core logic unit, or north bridge, as illustrated with reference to FIGS. 1 and 2 of Jeddeloh. Applicants respectfully submit that this north bridge is analogous to the I/O controller recited by Claim 19. However, the I/O controller, as recited by Claim 19, does not include an embedded graphics controller 140, as taught by Jeddeloh. Applicants respectfully submit that

Jeddeloh teaches away from a graphics controller coupled to north bridge 102, since such a modification would prohibit direct coupling between the graphics controller 140 and switch 124, as explicitly required by Jeddeloh.

As such, modification of Jeddeloh to include an intervening interface or a bus between graphics controller 140 and switch 124 could introduce bandwidth limitations, which would prohibit the stated goal of Jeddeloh of providing high-bandwidth communications between the graphics controllers and other computer system components, such as the processor and system memory. (*See*, col. 2, lines 19-21.) Yet, the case law clearly established that "it is improper to combine references where the references teach away from their combination. In re Grasselli, 713 F.2d 731, 743, 218 U.S.P.Q. 769, 779 (Fed. Cir. 1983). Accordingly, Applicants respectfully submit that the Examiner is prohibited from combining Jeddeloh in view of Alpert and further in view of Dixit since Jeddeloh teaches away from a graphics controller coupled to an I/O controller, as recited by Claim 19. Id.

In fact, Applicants submit that modification of Jeddeloh to teach an I/O controller, or north bridge, coupled to a graphics controller would run contrary to the explicit teachings of Jeddeloh. One of ordinary skill in the art would not be motivated to modify Jeddeloh in a manner specifically contrary to Jeddeloh's own teachings. Accordingly, Applicants' claimed invention could only be arrived at through inappropriate hindsight. Therefore, a *prima facie* case of obviousness of the claims is not established and the rejection of Claims 19-21 should be overturned.

E. Rejection of Claims 30-31 as Obvious Over Jeddeloh in View of Alpert

The Examiner rejected Claims 30-31 under 35 U.S.C. §103(a) as being unpatentable over Jeddeloh in view of Alpert.

1. Errors of Law and Fact in the Rejection

The Examiner has made the same errors as described previously with respect to the rejected Claims 6-9 and 12-14. In addition, the Examiner has failed to show a teaching or suggestion to modify Jeddeloh in view of Alpert. Applicants respectfully submit that Applicants' claimed invention could only be arrived at through inappropriate hindsight. Hence, a *prima facie* case of obviousness has not been established and the rejection is erroneous and should be overturned.

Furthermore, according to the Examiner, Jeddeloh inherently teaches a translation control circuit coupled to the address translator to program the entries in the address translator, as recited by the claimed invention. According to the Examiner:

> The address translator comprises interfaces and a table, wherein neither of these elements have logic to control the operation of the address translator and thus it is evident that logic is coupled to the address translator for controlling its operations such as storing, programming addresses/entries in the table. (*See*, ¶1, pg. 5 of the Final Office Action mailed July 14, 2004.)

Applicants respectfully submit that the Examiner cannot establish a *prima facie* case of obviousness since the passage above fails to provide a basis in fact under technical reasoning to reasonably support the determination that the alleged inherent characteristic necessarily flows from the teachings of the prior art. *Ex Parte* Levy, 17 U.S.P.Q. 2d 1461, 1464 (Bd. Pat. App. and Intr. 1990).

The Federal Circuit Court of Appeals of In Re Rijckaert, 9, F.3d 1531 (Fed. Cir. 1993) held that:

> [T]he fact that a certain result or characteristic may occur or be present in the prior art is not efficient to establish the inherency of that result or characteristic. (9 F.3d at 1534, 28 U.S.P.Q. 2d at 1955, 1957.)

Here, the claimed invention recites a control circuit to populate the address translator. Applicants respectfully submit that the Examiner has inappropriately relied on the inherency of a control circuit within Jeddeloh in spite of the failure to teach or suggest such a control circuit or any sort of logic for generating the GART table, initially creating the GART table or performing address translation using the GART table. Applicants respectfully submit that such failure is based on the fact that the teachings of Jeddeloh are not directed to the GART table and are, in fact, directed to enabling high-bandwidth communication between the various devices coupled to switch 124 within north bridge 102, as taught by Jeddeloh.

Accordingly, Applicants respectfully submit that the Examiner has failed to establish the inherency of the translation control circuit, as recited by the claimed invention, within the combination of Jeddeloh in view of Alpert. Hence, a *prima facie* case of obviousness has not been established and the rejection is erroneous and should be overturned.

2. Specific Limitations Not Described in the Prior Art

Independent Claim 30 recites the following claim feature, which is neither taught nor suggested by either Jeddeloh, Alpert or the references of record:

> a translation control circuit coupled to the address translator to program the entries in the address translator;
>
> wherein the address translator is to translate an address on the third interface into a first address on the first interface having a greater number of bits than the address on the third interface. (Emphasis added.)

3. Explanation Why Such Limitations Render the Claims Non-obvious Over the Prior Art

The case law is clear in establishing that to establish a *prima facie* case of obviousness of the claimed invention, all claim limitations must be taught or suggested by the prior art. In re Royka, 490 F.2d 981, 180 U.S.P.Q. 580 (CCPA 1974).

Here, Alpert is directed to modification of the paging mechanism of a processor to enable selection of a physical address range size and page size selection, which requires use of processor control registers, three levels of tables and various configurations of a linear address to include a pointer field 46, directory field 44, page field 46 and offset field 48 to provide the physical address range size and page size, as shown in FIGS. 2, 8, 10 and the flowcharts in FIGS. 11 and 12 of Alpert.

Applicants respectfully submit that using the teachings of Alpert with the teachings of Jeddeloh, as suggested by the Examiner, would result in the system as taught by Jeddeloh, in which the processor paging mechanism is altered without any modification to the address translation using the GART table. As indicated above, the inability of off-chip devices to make use of a processor's paging mechanism, and specifically, the graphics controllers, is the reason for the creation of the GART table to perform such translation for graphics devices.

Therefore, the teachings of Alpert are strictly limited to the modification of the processor paging mechanism. Consequently, Applicants respectfully submit that the combination of the teachings of Jeddeloh in view of Alpert would be limited to the modification of the processor paging mechanism of processors 112, 114 and 116, as illustrated in FIG. 1 of Jeddeloh. The case law is clear in establishing that to establish a *prima facie* case of obviousness of the claimed invention, all claim limitations must be taught or suggested by the prior art. In re Royka, 490 F.2d 981, 180 U.S.P.Q. 580 (CCPA 1974).

Accordingly, the combination or modification of Jeddeloh in view of Alpert would fail to teach or suggest address translation from a graphics controller and a bus controller using the same conversion table where a number of bits of the translated address is greater than a number of bits of the initial address, as recited by the claimed invention. Hence, the Examiner fails to establish a *prima facie* case of obviousness since the combination or modification of Jeddeloh in view of Alpert fails to teach all limitations of the claimed invention. Id.

Furthermore, Applicants respectfully submit that the Examiner cannot provide a basis in fact under technical reasoning to support the inherency of a translation control circuit coupled to the address translator to program entries in the address translator, as recited by the claimed invention. Applicants respectfully submit that the complete absence of any description of the address translation mechanism within Jeddeloh supports this conclusion. Furthermore, Applicants respectfully submit that as known to those skilled in the art, GART tables are conventionally formed using software.

Hence, Applicants respectfully submit that the Examiner is prohibited from relying on the inherent disclosure of a translation control circuit coupled to the address controller to program entries in the address translator, as recited by the claimed invention, because the Examiner has not complied with the requirements of rejections based on inherency. (*See*, M.P.E.P. §2112.) Applicants respectfully request that the rejection be overturned.

VIII. CONCLUSION AND RELIEF

Based on the foregoing, Applicants request that the Board overturn the rejection of all pending claims and hold that all of the claims of the present application are allowable.

Respectfully submitted,

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Dated: 11 | 30 , 2004

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CERTIFICATE OF MAILING:
I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail, with sufficient postage, in an envelope addressed to: Mail Stop Appeal Brief - Patents, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on November 30, 2004

Marilyn Bass 11 | 30 , 2004

IX. APPENDIX

The claims involved in this Appeal are as follows:

1-7 (Cancelled)

8. (Previously Presented) A method, comprising:

using a conversion table to translate a first address from a graphics controller to a second address to a memory; and

using the conversion table to translate a third address from a bus controller to a fourth address to the memory;

wherein the second address has a greater number of bits than the first address and the fourth address has a greater number of bits than the third address.

9. (Previously Presented) The method of claim 8, wherein said using the conversion table to translate the third address includes using a translation lookaside buffer.

10-11 (Cancelled)

12. (Previously Presented) The method of claim 8, wherein said using the conversion table to translate the third address includes:

comparing a first portion of the third address with entries in a first table;

if the first portion matches a particular one of the entries in the first table, combining a value associated with the particular one with a second portion of the third address to form the fourth address.

13. (Previously Presented) The method of claim 12, further comprising:

if the first portion does not match any of the entries in the first table, referring to a second table to translate the third address.

14. (Previously Presented) The method of claim 13, wherein:

said comparing includes comparing the first portion of the third address with entries in the first table in an input-output controller; and

said referring to the second table includes referring to the second table in main memory.

15. (Previously Presented) An apparatus, comprising:

a translation lookaside buffer coupled to an input register and an output register;

control logic coupled to the translation lookaside buffer, the input register, and the output register; wherein the control logic is to compare a first portion of an initial address from a bus controller in the input register with entries in the translation lookaside buffer; and if a matching entry is found, to combine a first value associated with the matching entry with a second portion of the initial address to form a first translated address having a greater number of bits than the initial address and hold the first translated address in the output register;

wherein the control logic is further to access a table in memory if the matching entry is not found, find a second value in the table associated with the first portion, combine the second value with the second portion to form a second translated address having a greater number of bits than the initial address, and hold the second translated address in the output register.

16. (Cancelled)

17. (Previously Presented) The apparatus of claim 15, wherein:

the control logic includes logic for first and second control flows;

the second control flow is to translate an initial graphics controller address and does not access the second table; and

the first control flow is to translate an initial bus controller address and access the second table.

18. (Cancelled)

19. (Previously Presented) A system, including:

a processor;

a memory;

a graphics controller;

a bus controller;

an input-output controller coupled to the processor, memory, graphics controller and bus controller, the input-output controller including:

a translation lookaside buffer coupled to an input register and an output register;

control logic coupled to the translation lookaside buffer, the input register, and the output register;

wherein the control logic is to compare a first portion of a first initial address from the bus controller in the input register with entries in the translation lookaside buffer; and if a first matching entry is found, to combine a first value associated with the first matching entry with a second portion of the first initial address to form a first translated address having more bits than the first initial address and hold the first translated address in the output register;

wherein the control logic is further to compare a first portion of a second initial address from the graphics controller in the input register with the entries in the translation lookaside buffer; and if a second matching entry is found, to combine a second value associated with the second matching entry with a second portion of the second initial address to form a second translated address having more bits than the second initial address and hold the second translated address in the output register.

20. (Previously Presented) The system of claim 19, wherein the control logic is further to:

access a table in memory if the first matching entry is not found;

find a third value in the table associated with the first portion of the first initial address;

combine the third value with the second portion of the first initial address to form a third translated address: and

hold the third translated address in the output register.

21. (Previously Presented) The system of claim 20, wherein:

the control logic includes logic for first and second control flows;

the second control flow is to translate an initial graphics controller address and does not access the table; and

the first control flow is to translate an initial bus controller address and access the table.

22-29. (Cancelled)

30. (Previously Presented) An apparatus comprising:

an address translator having a first interface to couple to a memory controller, a second interface to couple to a graphics controller, a third interface to couple to a bus controller, and a table of entries, each entry having a first portion and a second portion;

a translation control circuit coupled to the address translator to program the entries in the address translator;

wherein the address translator is to translate an address on the third interface into a first address on the first interface having a greater number of bits than the address on the third interface.

31. (Previously Presented) The apparatus of claim 30, wherein:

the address translator is further to translate an address on the second interface into a second address on the first interface having a greater number of bits than the address on the second interface.

32. (Previously Presented) The apparatus of claim 30, wherein:

the address translator comprises a graphics translation lookaside buffer.